Attorney Docket No. BU9-99-067 (21806-00070-US1) Application No. 10/672,012

## IN THE CLAIMS

This listing of claims will replace all previous versions and listings of claims in the application:

## LISTING OF CLAIMS

- 1-19 (Cancelled).
- 20. (Previously presented) A method for making a semiconductor chip comprising:

forming a diffusion region in a semiconductor substrate;

forming an insulated trench structure in said substrate which surrounds said diffusion region; and

forming electrical connections on said trench structure and said substrate which receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region.

- 21. (Previously presented) The method for making a semiconductor chip according to claim 20, further comprising source and drain regions formed in said diffusion on each side of a gate.
- 22. (Original) The method of making a semiconductor chip according to claim 20, wherein said diffusion region forms a resistor which has a resistance controlled in response to said control voltage.
- 23. (Previously presented) The method of making a semiconductor chip according to claim 20, wherein said diffusion region is formed in a well of polysilicon deposited in said trench structure.

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- 24. (Original) A method for making a semiconductor chip comprising: forming first and second diffusion regions in a semiconductor substrate; forming a trench structure around said first and second diffusion regions; and forming a contact on said trench structure and said substrate for controlling current through said diffusion regions.
- 25. (Original) The method for making a semiconductor chip according to claim 24, further comprising:

forming first and second gates over said first and second diffusion regions.

26. (Previously presented) A method for making a semiconductor chip comprising:

forming multiple diffusion regions that are surrounded by multiple trench structures on a substrate; and

forming multiple contacts on each of said trench structures and said substrate for controlling current through said diffusion regions.

27. (Original) The method for making a semiconductor chip according to claim 26, further comprising:

forming a gate electrode over each of said diffusion regions; and forming drain and source connections on opposite sides of said gate electrodes.